REMARKS

At pages 2-3 of the Office Action, the Examiner rejects claims 1, 4, 7, 10, 13 and 16 under 35 USC 103(a) as being unpatentable over Suzuki et al. (US Patent No. 6,043,145) in view of Kurauchi et al. (US Patent No. 6,323,921). Moreover, at pages 4-5, claims 2, 3, 5, 6, 8, 9, 11, 14, 15, 17 and 18 are rejected under 35 USC 103(a) as being unpatentable over Suzuki et al. in view of Kurauchi et al., and further in view of Lin et al. (US Patent No. 6,063,653). These rejections are respectfully traversed.

Suzuki et al., Kurauchi et al. and Lin et al., standing alone or in combination, does not disclose, *inter alia*, the following limitations of the claimed invention:

Claim 1: "forming on the substrate a plurality of signal lines along a first direction and a plurality of gate lines along a second direction to define a plurality of pixels, the first direction being perpendicular to the second direction, each pixel including a first area;

forming a switching unit in the first area of each pixel;

forming a first photoresist layer to cover a first group of the pixels;

forming a second photoresist layer to cover a second group of the pixels; and

forming a third photoresist layer to cover a third group of the pixels, wherein the first area of each pixel is covered by at least two of the first, second and third photoresist layers."

Claim 7: "a plurality of signal lines disposed on the glass substrate along a first direction and a plurality of gate lines disposed on the glass substrate along a second direction to define a plurality of pixels, the first direction being perpendicular to the second direction, each pixel including a first area;

a plurality of switching units disposed in the first areas of the pixels;

a first photoresist layer covering a first group of the pixels;

a second photoresist layer covering a second group of the pixels; and

a third photoresist layer covering a third group of the pixels,

wherein the first area of each pixel is covered by at least two of the first, second and third photoresist layers."

Claim 13: "a plurality of signal lines disposed on the first substrate along a first direction and a plurality of gate lines disposed on the glass substrate along a second direction to define a plurality of pixels, the first direction being perpendicular to the second direction, each pixel having a first area;

a plurality of switching units disposed in the first areas of the pixels;

a first photoresist layer covering a first group of the pixels;

a second photoresist layer covering a second group of the pixels; and

a third photoresist layer covering a third group of the pixels,

wherein the first areas of each pixel is covered by at least two of the first, second and third photoresist layers."

Suzuki et al. discloses a method for making a multilayer wiring structure. Suzuki et al. relates to a **technical area totally different** from that of the present application (relating to a flat panel display with a

color filter and TFTs disposed on the same substrate). Comparing the figures of Suzuki et al. with the figures of the present application, there is almost nothing in common between these two inventions, except that both have many different layers.

At page 2 of the Office Action, the Examiner asserts that in Suzuki, the insulating layers are etched (col. 6, lines 21-37) such that the insulating layers substantially function as resist layers. The Applicant could not find any indication in the cited passage that the insulating layers function as resist layers or photoresist layers. Moreover, where does Suzuki mention "a plurality of **pixels**", as recited by claims 1, 7 and 13 of the present application? Since Suzuki is not related to display or color filter, there seems to be no motivation to include photoresist layers or pixels in its structure.

There are many reasons that Suzuki's insulating layers do not read on the photoresist layers of the claimed invention. For example, in the present application, the first, second and third photoresist layers cover **three different groups of the pixels**. If the first, second and third insulating films (63, 64, 68) read on the first, second and third photoresist layers, the first, second and third insulating films (63, 64, 68) should cover three different regions. However, in Suzuki the first insulating film (63) and the second insulating film (64) cover the same region. Therefore, at least for this reason, it is not reasonable to read the first, second and third insulating films (63, 64, 68) on the first, second and third photoresist layers.

At page 2 of the Office Action, the Examiner acknowledges that Suzuki

does not disclose forming a plurality of signal lines and a plurality of gate lines that cross each other and forming a switching unit in each pixel area. However, he asserts that Kurauchi teaches that a matrix substrate includes plural scanning lines and plural signal lines intersecting with each other, switching elements (thin film transistors) at the intersecting regions, and pixel electrodes (col. 6, lines 34-38). The Applicant respectfully disagrees.

Kurauchi discloses a color filter substrate used for a liquid crystal display device. However, Kurauchi does not disclose a structure in which **both** the color filter and the black matrix are formed on the TFT array substrate, which is the objective of the present application (see page 2, lines 5-9). With respect to features of the present application, Kurauchi does not teach anything more than the admitted prior art described at pages 1-2 of the specification. In other words, Kurauchi only discloses forming a color filter on a substrate, not forming both the color filter and a black matrix on a TFT array substrate.

Kurauchi fails to disclose many elements of the claimed invention. For example, the Examiner does not show what part of Kurauchi teaches forming the three photoresist layers to cover **three different groups of pixels**, or that the first area of each pixel is covered by at least two of the first, second and third photoresist layers, as recited by claims 1, 7 and 13 of the present application.

Liu et al. discloses patterning a metal layer on a glass substrate. Comparing figures of Liu et al. to figures of the present application, it is obvious that the structure in Liu et al. is very different from that of the

present application. For example, the Examiner does not show what part of Liu et al. teaches forming the three photoresist layers to cover three different groups of pixels, or that the first area of each pixel is covered by at least two of the first, second and third photoresist layers, as recited by claims 1, 7 and 13 of the present application.

Under MPEP 2143, "[t]he teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure" (citing In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)). The Applicant believes that the combination of Suzuki et al., Kurauchi et al. and Lin et al. is not based on any suggestions in the prior art, but based on a hindsight reconstruction of the claims in the present application. There is no motivation or suggestion to combine the cited references, which belong to very different technical fields. Moreover, even if these references are combined, they do not teach all limitations of the claimed invention, as discussed above.

In summary, the Applicant believes that claims 1, 7 and 13 are patentable over the cited references. Claims 2-6, 8-12 and 14-18 are also patentable, at least by virtue of their dependency from claim 1, claim 7 or claim 13.

The Applicant believes that all claims are in condition for allowance and reconsideration of the present application is respectfully requested.

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particular, if this response is not timely filed, then the Commissioner is authorized to treat this response as including a petition to extend the time period pursuant to 37 CFR 1.136 (a) requesting an extension of time of the number of months necessary to make this response timely filed and the petition fee due in connection therewith may be charged to deposit account no. 12-0415.

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7/21/2003
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